BBP-100 BINARY BIT PROCESSOR

MARK II REVISION B

Dovetron provides two types of the Binary Bit Processor in the Mark II versions of the Dovetron terminal unit.

Both are considered to be current production and are interchangeable, although the Revision B units offer additional features as noted below.

The earlier BBP-100 is identified by the board number 75193 REV A. The corresponding prints are Assembly 75192 and Schematic 75195. The later BBP-100 is assembled on board number 75350 REV B and the corresponding Assembly/Schematic print is combined on Print 75349B.

In addition to the BBP functions of Bandwidth Selection, Low Pass Filtering, Axis Restoration and Multipath Correction, the Revision B unit also provides an AFSK Tone Monitor circuit and an AFSK Tone Control section.

The CA-9160 cable assembly must be installed in the main frame of the Dovetron terminal unit to utilize the AFSK Tone Monitor and the AFSK Tone Control features.

When the Revision B unit is factory-installed, the CA-9160 cable assembly is normally installed in the main frame, if the Monitor/Control circuits are to be utilized.

Both versions of the BBP-100 permit front-panel switch-selection of three different bandwidths, which are tailored to provide optimum operation at three different baud rates.

These bandwidths (baud rates) are predetermined by the resistor values of three separate plug-in bandwidth modules: NARROW, MEDIUM & WIDE.

The factory normally provides modules for 50, 75 and 110 baud.

Since only resistive elements are switched when changing bandwidth, the bandwidth of the terminal unit may be changed during operation without interrupting the data thru-put or creating errors.

Storage sockets are provided in the left-rear corner of the BBP units for additional bandwidth modules and/or spare module headers.

OPERATION: REVISION B

Reference Print 75349B, the Mark and Space signals from the

terminal unit's Precision Detectors and Diversity Combiner circuits enter the BBP-100 assembly thru Z24-3 (Mark) and Z16-3 (Space) and are combined at pin 3 of op-amp U4.

The Low Pass Filter consists of U6 and U7 and their associated components.

The resistive elements of this four pole low pass filter are selected by three CMOS 14066 bilateral switches U1, U2 and U3.

Selectable bandwidth is achieved by enabling either U1 (Narrow), U2 (Medium) or U3 (Wide). The control logic for this selection is provided by U5, which is connected to the front panel three-position Bandwidth switch via the interconnecting circuitry of Z26-3, Z27-2 and Z29-2.

When the Bandwidth switch is in the Narrow position, Z27-2 is high (+7 VDC), and the U1 is enabled, providing a Narrow bandwidth.

With the Bandwidth switch in the Wide position, Z29-2 is high, and U3 is enabled, providing a Wide bandwidth.

If neither line is high, i.e., both are low, U5 provides an enable command to U2, which provides the Medium bandwidth selection.

Axis Restoration and Multipath Correction are provided by U8, U9, U10 and U11.

Optimum performance of these circuits is achieved by matching the timing characteristics of U8 and U9 with the incoming baud rate, i.e., by varying the values of resistance at R5 and R6.

As the bandwidth of the low pass filter is selected by the front panel Bandwidth switch, U10 selects the proper value for R5 and R6.

The dual inputs to the first two sections of U11 provide Multipath Correction for signals with apparent pulse stretching.

The third section of U11 provides a fully-processed FSK signal to the mainboard of the terminal unit thru interconnect point Z36-6.

The fourth section of U11 functions as an inverter, and provides the necessary inverted FSK data for use in the TEMPEST versions of the Dovetron terminal unit.

The -400 MV signal outputted thru Z26-6 drives the automatic Markhold, Threshold, Autostart and Signal Loss circuits on the terminal unit's mainboard.

AFSK TONE MONITOR

A 14066 bilateral switch U12 permits the output of the AFSK Tone Keyer to be routed back into the front end of the terminal unit whenever the terminal unit is in the half-duplex SEND mode.

This function provides a visual indication in the SSD-100 Solid State Cross Display (U. S. Patent 4229698) as the AFSK Tone Keyer is keyed and the Mark and Space tone frequencies are transmitted.

A similar AFSK Tone Monitor is provided on the KOS-100 Keyboard Operate Send assembly. If the KOS-100 is installed in the terminal unit, the AFSK Tone Monitor on the BBP-100 is normally disabled by removing the 14066 bilateral switch chip at U12.

AFSK TONE CONTROL

A second 14066 bilateral switch at U13 permits operator-selection of outputting the tones from the AFSK Tone Keyer continuously or only when the terminal unit is in the SEND (XMIT ONLY) mode.

The XMIT ONLY mode permits a companion VOX-operated transceiver to be switched between Receive and Transmit by the tones from the terminal unit.

VARIATIONS

Provision has been on the BBP board to permit the use of plug-in modules for the various combinations of resistors at R5 and R6 in the Axis Restoration-Multipath Correction section.

Unless specified at time of ordering, Dovetron provides discrete resistors at R5W, R5M, R5N, R6W, R6M and R6N that match the baud rate requirements of the bandwidth modules (Narrow, Medium and Wide) and their resistors R1, R2, R3 and R4.

TESTING AND TROUBLE SHOOTING

Check supply voltages at the test points on the BBP-100: +15, -15, +7 and -7 VDC. These voltages are regulated by the ±15 VDC regulators on the terminal unit's mainboard.

If one or more of the voltages appears to be low, attempt to locate the component that is pulling the supply down.

The five 14066 I.C.s are CMOS and should not be warm to the touch. Any heat generated in a CMOS chip generally indicates a defective chip.

The op-amps (μ741CP, TL081CP and TL084/LM324) consume power and will be warm to the touch. If shorted, op-amps tend to break open and sometimes run hot enough to melt the plastic socket underneath.

If one of the bandwidth positions is not functioning, suspect a bad 14066 bilateral switch or a poor solder connection between the resistor and the pin on a bandwidth module.

TEST POINT MEASUREMENTS

Test points N, M and W normally set a -7 VDC, and individually switch to +7 VDC depending on the position of the front panel Bandwidth switch. When WIDE is selected, Test Point W will be +7 VDC, and the M and N will be at -7 VDC, etc.

With no signal input, the front panel Mode switch at MS, and the Threshold Control set nominally to 12 o'clock:

TP1, TP2, TP3, TP4, TP5 and TP6: Zero output.

TP7: -14 VDC. TP8: +14 VDC. TP9: -400 MV nominal.

With Mode Switch set for MS-REV, Mark and Space VFOs tuned to correct Mark and Space tone frequencies, LEVEL and THRESHOLD controls set for 12 o'clock, and normal display in SSD-100 Cross Display:

TP1: Combined output from precision detectors on mainboard with carrier frequencies still present on Mark and Space levels. Voltage levels approximately ±6 VDC. Indicates that U4 is functioning correctly.

TP2: Output of first stage of low pass filter. Carrier frequencies are stripped from data and front panel Bandwidth control will modify appearance of signal. When baud rate of RY Generator (MS-REV) is set for same bandwidth as front panel switch, signal will appear to be a sine wave. If the Bandwidth switch is set for a wider bandwidth than the RY Generator, the signal will have a tendency to "square-up" and lose its smoothness. (See TP3 below.)

TP3: Output of the second stage of the low pass filter. Characteristics same as at TP2. No output at either TP2 or TP3 indicates problem with Low Pass Filter U6 or U7, or with Bandwidth selection chips U1, U2 or U3, and/or Bandwidth Modules W, M or N.

TP4: Output of positive section of Axis Restorer. Output level of +3 to +5 VDC, ramping at baud rate, and displaying discharge of C7. Voltage increases slightly as bandwidth is increased, i.e., as switched from Narrow, thru Medium, to Wide. Faulty component may be U8 or C7.

TP5: Output of negative section of Axis Restorer. Output level of -3 to -5 VDC, ramping at baud rate, and displaying discharge of C8. Voltage increases slightly as bandwidth is increased, i.e., as switched from Narrow, thru Medium, to Wide. Faulty component may be U9 or C8.

TP6: Combined output of Axis Restorer-Multipath Corrector. Resembles sine wave with perfect zero crossing of baud rate of RY Generator is similar to bandwidth setting.

TP7: FSK output from Slicer U11. ±14 VDC square wave. Mark low and Space high. Suspect U11 as faulty if output is not square wave.

TP8: Same as TP7, but inverted. Mark high and Space low.

TP9: ±3 VAC Sine Wave. Smooth when baud rate of RY Generator is similar to bandwidth setting. Squares up if bandwidth is wider than optimum. This sine wave has a nominal -400 MV offset. Offsets between -200 MV and -400 MV are acceptable. R17 and R18 function as a voltage divider to determine the amount of offset.

AFSK TONE MONITOR CIRCUIT

J1-6: This test point monitors the status of the Send-Receive line in the terminal unit. It is the cathode of CR52 on the mainboard. CR52 is not normally installed. The cathode end of CR52 is connected to the cathode end of CR55, which is driven high when the terminal unit is in the SEND mode.

In Receive, with the RY Generator functioning, some positive ripple may be on the line. This is okay. With the RY Generator turned off, J1-6 will be zero volts.

In Send, with or without RY Generator functioning, J1-6 will be high, i.e., +14 to +15 VDC.

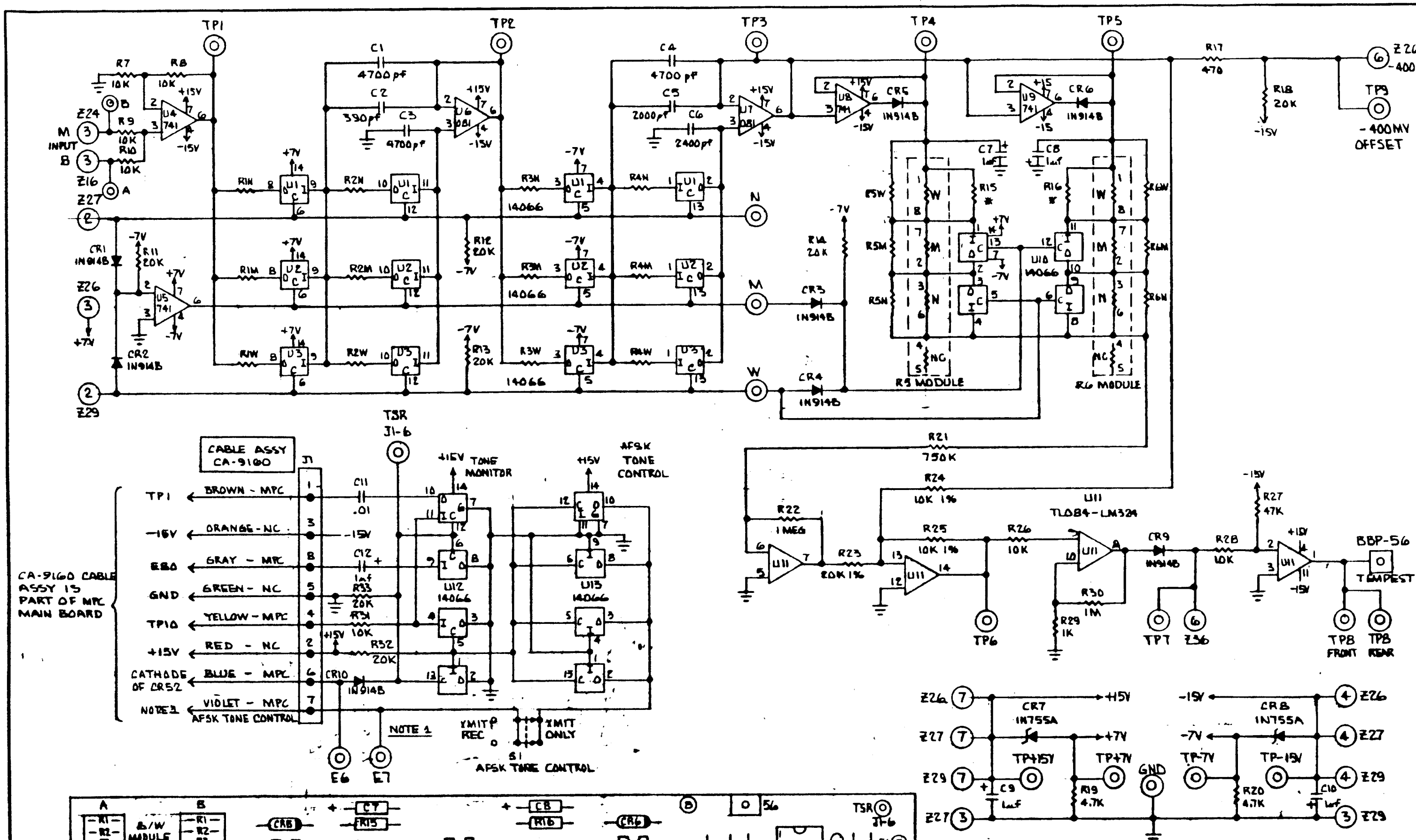
If AFSK Tone Monitor circuit does not function, replace the 14066 at U12. This chip can be damaged by allowing excessive RF to enter the terminal unit thru the 600 ohm Audio Input connector on the rear panel.

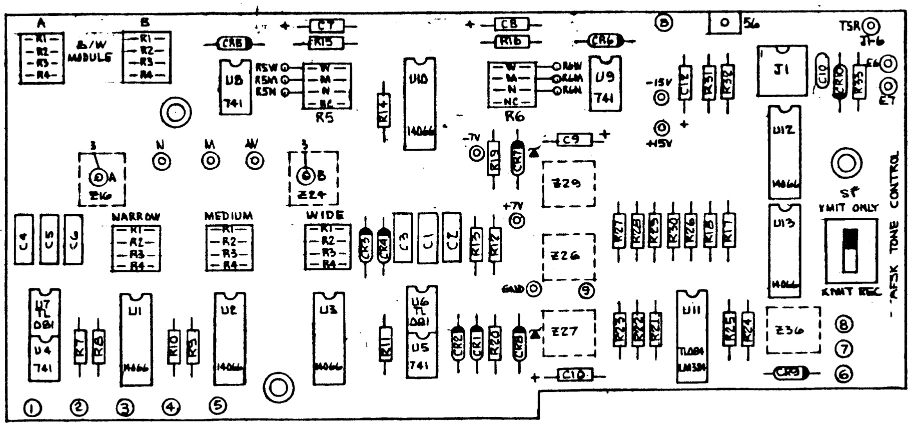
AFSK TONE CONTROL CIRCUIT

If this circuit does not function, replace the 14066 at U13. Check XMIT-REC/XMIT-ONLY switch for proper function. Contacts may be cleaned by rapid switching back and forth manually.

NOTE: The AFSK TONE MONITOR and AFSK Tone Control sections of the BBP-100 are not always installed, depending on customer requirements and the installation of other Dovetron options. In some units, these functions may be installed, but the CA-9160 interconnect cable may be missing, again depending on the customer's requirements and the terminal unit's configuration.

Both are to be considered options, and in no way affect the proper operation of the signal processing sections of the BBP-100 Binary Bit Processor.





	R5-R6 MODULES				
	R	BAUD		R	BAUD
W	75K	150		100K	100 110
M	75K	75		75K	75
N	75K	50		75K	45
N/C	100K	---		75K	---
W	36K	300		150K	75
M	36K	150		75K	50
N	24K	110		24K	45
N/C	---	---		---	---
W	18K	600		18K	600
M	18K	300		18K	300
N	36K	150		62K	110
N/C	---	---		---	---

LOW PASS FILTER	
BAUD RATE BANDWIDTH	
BAUD	R1-R4 RES
45.45	820K
50.00	750K
56.88	680K
74.20	510K
75.00	510K
100.00	360K
110.00	330K
150.00	240K
300.00	130K
600.00	62K

MARK II

TONE MONITOR SECTION

With U12 (14066) installed and J1 Cable Assembly connected to mainboard, the AFSK tone keyer output tones will be displayed in the ESD Cross Display when terminal unit is in the Transmit (half-duplex) mode.

AFSK TONE CONTROL SECTION

If U13 (14066) is also installed, the AFSK tone keyer output may be inhibited during Receive and enabled when the terminal unit is in Transmit.

Reference Note 1:

Connect J1-7 (violet):

MPC-1000CR and MPC-1000R: AFSK output connector.

MPC-1000C/DK and MPC-1000CR/DK: Junction of R148 and R149. R149 is not installed in C/DK and CR/DK units.

MPC-1000T II: Rear-most R149 location. Front panel AFSK-OFF switch must be in UP (AFSK ON) position.

For AFSK Tone Control, both U12 and U13 must be installed. If only AFSK Tone Control is required, E6 and E7 may be hard-wired to the main board in lieu of using the 8 wire CA-9160 cable assembly.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

ITEM	QTY	PART NO.	REF. DESIG.	DESCRIPTION	MFR.
37	1	C56206L2	S1	SWITCH, SLIDE, DPDT, PC	SWITCHCRAFT
36					
35	5	CA-08PF-11	RES. MODULES	HEADER, 8PIN, BIFURCATED	CA
34	2	CA-16SLP-105D	U4,5,6,7	IC SOCKET, 16 PIN, LOW PROF	CA
33	7	CA-14SLP-105D	U1,2,3,10-13	IC SOCKET, 14 PIN, LOW PROF	CA
32	2	CA-8SLP-105D	U8,9	IC SOCKET, 8 PIN, LOW	CA
31	6	CA-08P-11	W,M,N,R5,R6,J1	IC SOCKET, 8 PIN, HIGH	CA
30	6	CA-08PF-11	Z16,24,26,27,29,36	HEADER, 8 PIN	CA
29					
28	1	TL084 LM324	U11	IC, QUAD OP-AMP	T.I. NATIONAL
27	4	741	U4,5,8,9	IC, MINI-DIP, OP-AMP	T.I.
26	2	TL081	U6,7	IC, MINI-DIP, OP-AMP	T.I.
25	6	14066	U1-3,10,12,13	IC, QUAD BILATERAL SWITCH	MOTOROLA
24	1	METAL FILM	R23	RESISTOR, 20K, 1%	DALE
23	2	METAL FILM	R24,25	10K, 1%	DALE
22	2	CARB FILM	R22,30	1M, 1/4W, 5%	R-OHM
21	1		R21	750K	
20	1		R27	47K	
19	7		R11-14,18,32,33	20K	
18	7		R7-10,26,28,31	10K	
17	2		R19,20	4.7K	
16	1		R29	1K	
15	1	CARB FILM	R17	RESISTOR, 470Ω 1/4W 5%	R-OHM
14					
13					
12	2	1N755A	CR7,8	DIODE, ZENER, 7.5V	ITT
11	8	1N914B	CR1-6,9-10	DIODE, SIGNAL, SIL.	IRC
10					
9					
8	5	TANTALUM	C7-10,12	CAPACITOR, 1uF, 35V	SPRAGUE
7	1	CER DISC	C11	.01uF	DILECTRON
6	1	DM15	C2	390 pf	C.D.
5	1	DM19	C5	2000 pf	C.D.
4	1	DM19	C6	2400 pf	C.D.
3	3	J630	C1,3,4	CAPACITOR, 4700 pf	PLESSY
2	1	CA9160	PART OF MPC MAIN BOARD	CABLE ASSY	C.A.
1	1	75350B	BBP-100 II	P.C. BOARD	DOVETRON

PARTS LIST

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS	DATE
DRAWN RO	2/27/85
CHECKED	
	1/84

DOVETRON
627 FREMONT AVE
SO PASADENA CA

BBP-100
BINARY BIT PROCESSOR

SCALE 2:1 | SIZE D | DRAWING NO. 75349 | B

DO NOT SCALE DRAWING | SHEET 1 OF 1